IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Jonghee Han

Serial No.: 10/716,079

Confirmation No.: 4850

Filed: November 18, 2003

For: LOW RISE/FALL SKEWED INPUT BUFFER COMPENSATING PROCESS VARIATION

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Group Art Unit: 2819

Examiner: Daniel D. Chang

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Commissioner for Patents
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Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

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July 12, 2006 /Christopher T. Shannon/
Date Christopher T. Shannon

RESPONSE TO FINAL OFFICE ACTION DATED MAY 12, 2006

In response to the Final Office Action dated May 12, 2006, having a shortened statutory period for response set to expire on August 12, 2006, please enter this response and reconsider the claims pending in the application for reasons discussed below. While no fees are believed due, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 20-0782 / INFN/SZ0028 / GGM for any fees, including extension of time fees or excess claim fees, required to make this response timely and acceptable to the Office.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper. Remarks/Arguments begin on page 10 of this paper.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Cancelled)

2. (Previously Presented) A method of reducing skew between rising and falling data at an output node of a buffer circuit, comprising:

generating an intermediate voltage signal from an input voltage signal applied to an input node of the buffer circuit;

generating an output voltage signal at the output node based on the intermediate voltage signal; and

coupling a first compensating current source between a supply voltage line and the output node to compensate for changes in NMOS current drive, wherein the first compensating current source comprises a current source transistor for delivering a compensating current to the output node, the current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

3. (Previously Presented) The method of claim 2, further comprising coupling a second compensating current source between the output node and ground to compensate for changes in PMOS current drive.

4. (Currently Amended) A method of reducing skew between rising and falling data at an output node of a buffer circuit, comprising:

generating an intermediate voltage signal from an input voltage signal applied to an input node of the buffer circuit;

generating an output voltage signal at the output node based on the intermediate voltage signal;

coupling at least one compensating current source to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged; and

controlling the amount of current provided by the compensating current source via a process dependent current source whose current is mirrored to the output node by the compensating current source.

5. (Original) The method of claim 4, further comprising controlling the amount of current supplied by the compensating current source via a relatively process independent bias voltage applied to a gate of a transistor of the process dependent current source.

6. (Cancelled)

7. (Cancelled)

8. (Previously Presented) A buffer circuit, comprising:

a first stage for generating an intermediate voltage signal from an input voltage signal applied to an input node of the first stage;

a second stage to receive the intermediate voltage signal and generate, on an output node of the second stage, an output voltage based on the intermediate voltage signal; and

at least a first compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the first compensating current source comprises a first current source transistor to supplement current flowing into the output node through the PMOS transistor as function of NMOS current drive, the first current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

9. (Original) The buffer of claim 8, wherein changes in current provided by the first current source are proportional to changes in current through the NMOS transistor.

10. (Original) The buffer circuit of claim 8, further comprising at least a second current source to supplement current flowing from the output node through the NMOS transistor as function of PMOS current drive.

11. (Currently Amended) A buffer circuit, comprising:

a first stage for generating an intermediate voltage signal from an input voltage signal applied to an input node of the first stage;

a second stage to receive the intermediate voltage signal and generate, on an output node of the second stage, an output voltage based on the intermediate voltage signal; and

at least a first compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the first compensating current source comprises a first current source transistor, a current flowing through the first current source transistor supplementing a ~~supplements~~ current flowing from the output node through the NMOS transistor as function of PMOS current drive, the first current source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

12. (Original) The buffer of claim 11, wherein changes in current provided by the first compensating current source are proportional to changes in current through the PMOS transistor.

13. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor; and

at least a first current mirror circuit having a first branch and a second branch coupled to the output node, the second branch delivering a current to the output node, wherein current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch.

14. (Previously Presented) The buffer circuit of claim 13, wherein:

current flowing through the first branch of the first current mirror circuit varies with changes to the NMOS current drive; and

current flowing from the second branch of the first current mirror circuit supplements current flowing into the output node through the PMOS transistor.

15. (Previously Presented) The buffer circuit of claim 13, wherein:

current flowing through the first branch of the first current mirror circuit varies with changes to the PMOS current drive; and

current flowing into the second branch of the first current mirror circuit supplements current flowing from the output node through the NMOS transistor.

16. (Original) The buffer of claim 15, further comprising at least a second current mirror circuit having a first branch and a second branch coupled with the output node, wherein:

current flowing through the first branch of the second current mirror circuit varies with changes to NMOS current drive; and

current flowing from the second branch of the second current mirror circuit supplements current flowing into the output node through the PMOS transistor.

17. (Original) The buffer circuit of claim 13, wherein the current flowing through the first branch of the first current mirror circuit is set by a process independent bias voltage supplied to a gate of a process dependent transistor.

18. (Original) The buffer circuit of claim 13, wherein the second branch of the first current mirror circuit comprises an NMOS transistor in parallel with the NMOS transistor of the inverter stage.

19. (Original) The buffer circuit of claim 13, wherein the second branch of the first current mirror circuit comprises a PMOS transistor in parallel with the PMOS transistor of the inverter stage.

20. (Cancelled)

21. (Cancelled)

22. (Previously Presented) A memory device, comprising:

an input to receive an external clock signal; and

a buffer circuit for generating an internal clock signal to be provided to one or more components of the memory device, wherein the buffer circuit comprises a first stage for generating an intermediate voltage signal indicative of a difference between a reference voltage signal and the clock signal, a second stage for generating an output voltage signal on an output node based on the intermediate voltage signal, an inverter for generating the internal clock signal based on the output voltage signal, and at least one compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the at least one compensating current source comprises a first current source transistor to supplement current flowing into the output node through the PMOS transistor as function of NMOS current drive, the first current

source transistor having a control terminal which is controlled independent of the intermediate voltage signal.

23. (Original) The memory device of claim 22, wherein the at least one compensating current source further comprises a second current source to supplement current flowing from the output node through the NMOS transistor as function of PMOS current drive.

24. (Currently Amended) A memory device, comprising:

an input to receive an external clock signal; and

a buffer circuit for generating an internal clock signal to be provided to one or more components of the memory device, wherein the buffer circuit comprises a first stage for generating an intermediate voltage signal indicative of a difference between a reference voltage signal and the clock signal, a second stage for generating an output voltage signal on an output node based on the intermediate voltage signal, an inverter for generating the internal clock signal based on the output voltage signal, and at least one compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and wherein the at least one compensating current source comprises a first current source transistor, a current flowing through the first current source transistor supplementing ~~to supplement~~ current flowing from the output node through the NMOS transistor as function of PMOS current drive, the first current source transistor having a control terminal which is controlled independent on the intermediate voltage signal.

25. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor;

at least a first current mirror circuit having a first branch and a second branch coupled to the output node, wherein:

current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch,

wherein current flowing through the first branch of the first current mirror circuit varies with changes to the PMOS current drive, and

wherein current flowing into the second branch of the first current mirror circuit supplements current flowing from the output node through the NMOS transistor; and

at least a second current mirror circuit having a first branch and a second branch coupled with the output node, wherein:

current flowing through the first branch of the second current mirror circuit varies with changes to NMOS current drive; and

current flowing from the second branch of the second current mirror circuit supplements current flowing into the output node through the PMOS transistor.

26. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor; and

at least a first current mirror circuit having a first branch and a second branch coupled to the output node,

wherein current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch, and

wherein the second branch of the first current mirror circuit comprises an NMOS transistor in parallel with the NMOS transistor of the inverter stage.

27. (Previously Presented) A buffer circuit, comprising:

a differential amplifier stage for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor and at least one NMOS transistor; and

at least a first current mirror circuit having a first branch and a second branch coupled to the output node,

wherein current flowing through the first branch is dependent on changes in at least one of NMOS or PMOS current drive and current flowing through the second branch mirrors the current flowing through the first branch,

wherein the second branch of the first current mirror circuit comprises a PMOS transistor in parallel with the PMOS transistor of the inverter stage.

REMARKS

This is intended as a full and complete response to the Final Office Action dated May 12, 2006, having a shortened statutory period for response set to expire on August 12, 2006. Applicant submits this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 2-5, 8-19 and 22-27 are pending in the application. Claims 2-5, 8-19 and 22-27 remain pending following entry of this response. Claims 4, 11, and 24 have been amended. Applicant submits that the amendments do not introduce new matter.

Claim Rejections - 35 U.S.C. § 102

Claims 2-5, 8-15, 17, and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by *Kiehl* (US 6,492,836 B2).

Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Kiehl* does not disclose "each and every element as set forth in the claim". For example, with respect to claims 2, 8, 22 and their dependents, *Kiehl* does not disclose "a current source transistor for delivering a compensating current to the output node, the current source transistor having a control terminal which is controlled independent of the intermediate voltage signal."

The Examiner argues that four transistors 226, 228, 230 and 232 in *Kiehl* are the current source transistors recited in the claims. However, the control electrodes of the transistors 226 and 228 are dependent on the voltage present at node 220, which was identified by the Examiner to carry the intermediate voltage signal. (See *Kiehl*, Figure 2A). Thus, transistors 226 and 228 cannot be current source transistors as recited in

the claims, because transistors 226 and 228 are dependent on the intermediate voltage signal. Therefore, transistors 226 and 228 are not current source transistors within the meaning of the claims.

Furthermore, the Examiner argues that transistors 230 and 232 are current source transistors according to the claims. The Examiner also argues that the node designated as OUT in Figure 2A of *Kiehl* is equivalent to the output node in the claims. However, the transistors 230 and 232 are not connected to the OUT node, rather transistors 230 and 232 are connected to the gate terminals of transistors 226 and 228, and therefore are isolated from the OUT node. (See *Kiehl*, Figure 2A). Thus, contrary to the requirements of the claim, transistors 230 and 232 are not used "for delivering a compensating current to the output node"; rather, transistors 230 and 232 are merely used to trigger or "turn-on" transistors 226 and 228.

The Examiner further argues that the transistor 230 of *Kiehl* delivers a compensating current "across" transistor 226 to the OUT node of Figure 2B. Applicant respectfully disagrees. The transistor 230 is connected to the gate terminal of transistor 226. (See *Kiehl*, Figure 2A) Although the drain of transistor 226 is connected to the OUT node, it is commonly known to one skilled in the art that a current, such as that delivered by transistor 230, cannot flow "across" the gate of a field effect transistor to the drain of the field effect transistor. Thus, transistor 226 does not deliver the current provided by transistor 230 at the gate of transistor 226 to the OUT node, because the current from transistor 230 is isolated from the OUT node by the gate of transistor 226. Therefore, it is believed that the statement that the current source transistor 230 delivers a compensating current "across" transistor 226 to the output node is not technically justified in view of the fact that transistor 226 is a field effect transistor having an isolated gate electrode.

Therefore, claims 2, 8, 22 and their dependents are believed to be allowable, and allowance of the claims is respectfully requested.

Regarding claim 13, *Kiehl* does not disclose "each and every element as set forth in the claim". For example, with respect to claim 13 and its dependents, *Kiehl* does not

disclose "a first current mirror circuit having a first branch and a second branch coupled to the output node, the second branch delivering a current to the output node."

The Examiner argues that transistor 230 may be considered the second branch of a current mirror, the first branch being shown in Figure 2C of *Kiehl*. Furthermore, the Examiner argues that mirrored current from transistor 230 is delivered to the OUT node, via transistor 226. Applicant respectfully disagrees. As stated above, the drain of transistor 230 is connected to the gate of transistor 226. (See *Kiehl*, Figure 2A) Thus, the current from the mirror circuit is not delivered to the output node, rather the mirror circuit current in *Kiehl* is merely used to trigger transistor 226. Therefore, *Kiehl* does not teach the claim limitation of "a first current mirror circuit having a first branch and a second branch coupled to the output node, the second branch delivering a current to the output node."

Therefore, claim 13 and its dependents are believed to be allowable, and allowance of the claims is respectfully requested.

Regarding claim 4 as amended, *Kiehl* does not disclose "each and every element as set forth in the claim". Furthermore, Applicant notes that the amendments have been made solely for the purposes of clarification and introduce recitations already present in other unamended claims. Accordingly, further search or consideration is not believed to be necessary.

With respect to claim 4, *Kiehl* does not disclose a "current is mirrored to the output node by the compensating current source." The Examiner argues that a current mirror is disclosed in *Kiehl* in Figure 2C in conjunction with transistor 230. Even if the circuit consisting of the transistor 230 and the circuit in Figure 2C is considered a current mirror, a current provided by the resulting circuit is not mirrored to the output node as recited by claim 4. Rather, the drain of transistor 230 is connected to the gate of transistor 226. Therefore, the current from transistor 230 is isolated from the OUT node by the gate of transistor 226. Thus, the current from transistor 230 is not "mirrored to the output node by the compensating current source" as required by the claim language; rather, any current or signal from transistor 230 is merely used to trigger or "turn on" transistor 226.

Therefore, claim 4 and its dependent claim 5 are believed to be allowable, and allowance of the claims is respectfully requested.

Regarding claims 11 and 24 as amended, *Kiehl* does not disclose "each and every element as set forth in the claim". Furthermore, Applicant notes that the amendments have been made solely for the purposes of clarification and introduce recitations already present in other unamended claims, therefore no further search is necessary.

With respect to claims 11 and 24, *Kiehl* does not disclose a "wherein the first compensating current source comprises a first current source transistor, a current flowing through the first current source transistor supplementing a current flowing from the output node through the NMOS transistor as a function of PMOS current drive, the first current source transistor having a control terminal which is controlled independent of the intermediate voltage signal." As presented in the arguments above with respect to claims 2, 8, and 22, nowhere in *Kiehl* is a current source transistor disclosed which supplements current flowing from the output node and is controlled independent of the intermediate voltage signal.

Therefore, claims 11 and 24 are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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